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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2024**

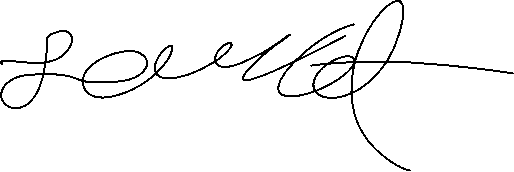
**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Logan Current**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Date: 10/30/2024**



**Report due date: 10/30/2024**

1. **OBJECTIVE**

The Objective of this lab is to make an XOR2 gate to use it to make a 1-bit full adder and then make a 2-bit full adder from that in Cadence Vivado.

1. **PROCEDURE**

Luckily, I made the XOR2 last lab, so, it was one less thing to do and all I needed to do was make the 1-bit FA and then implement a 2-bit FA.

First, I copied the 1-bit FA truth table then simplified both output equations to see how I should design this schematic. After figuring out what I needed to do to make the 1-bit FA I started to test and make the schematic using the NAND2 and XOR2 that I made in the previous labs and made the 1-bit FA. Then, I tested the schematic by outputting a waveform and confirming it matched the truth table that I had made, I calculated the propagation delay as well as the average output.

After that, making the 2-bit FA was easy. I just connected 2 of the 1-bit FA’s that I made and then started to test and output a waveform. I confirmed that it was outputting the correct output, I calculated the propagation delay and the average output of this gate.

1. **RESULT**

The order for the screenshots will be my written work first, then the gates. For each gate, the first screenshot will be schematic and then waveform.

A notebook with writing on it

Description automatically generatedA close-up of a paper

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XOR2:A computer screen shot of a computer program

Description automatically generatedA screenshot of a computer

Description automatically generated

1. Bit FA:

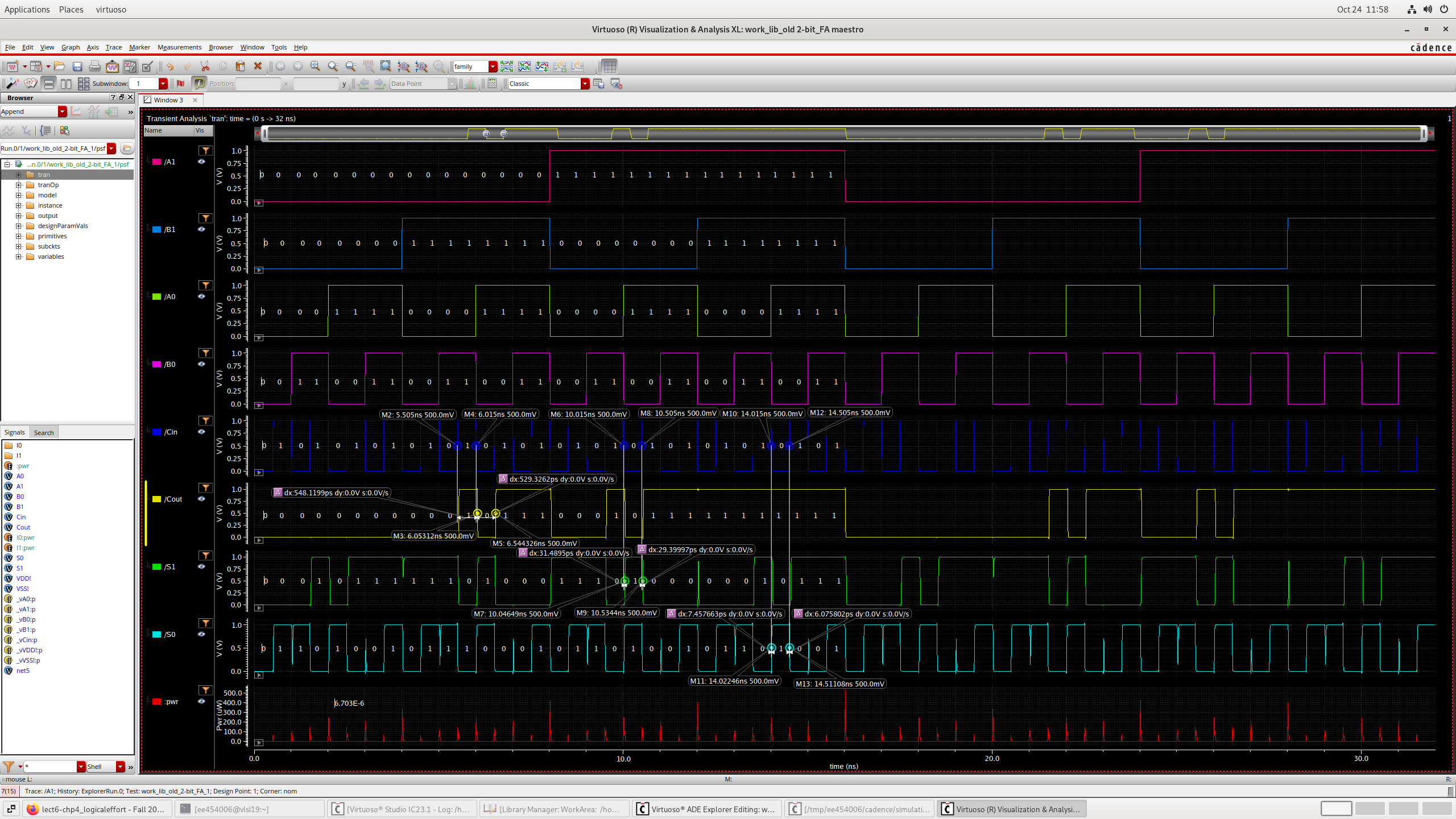
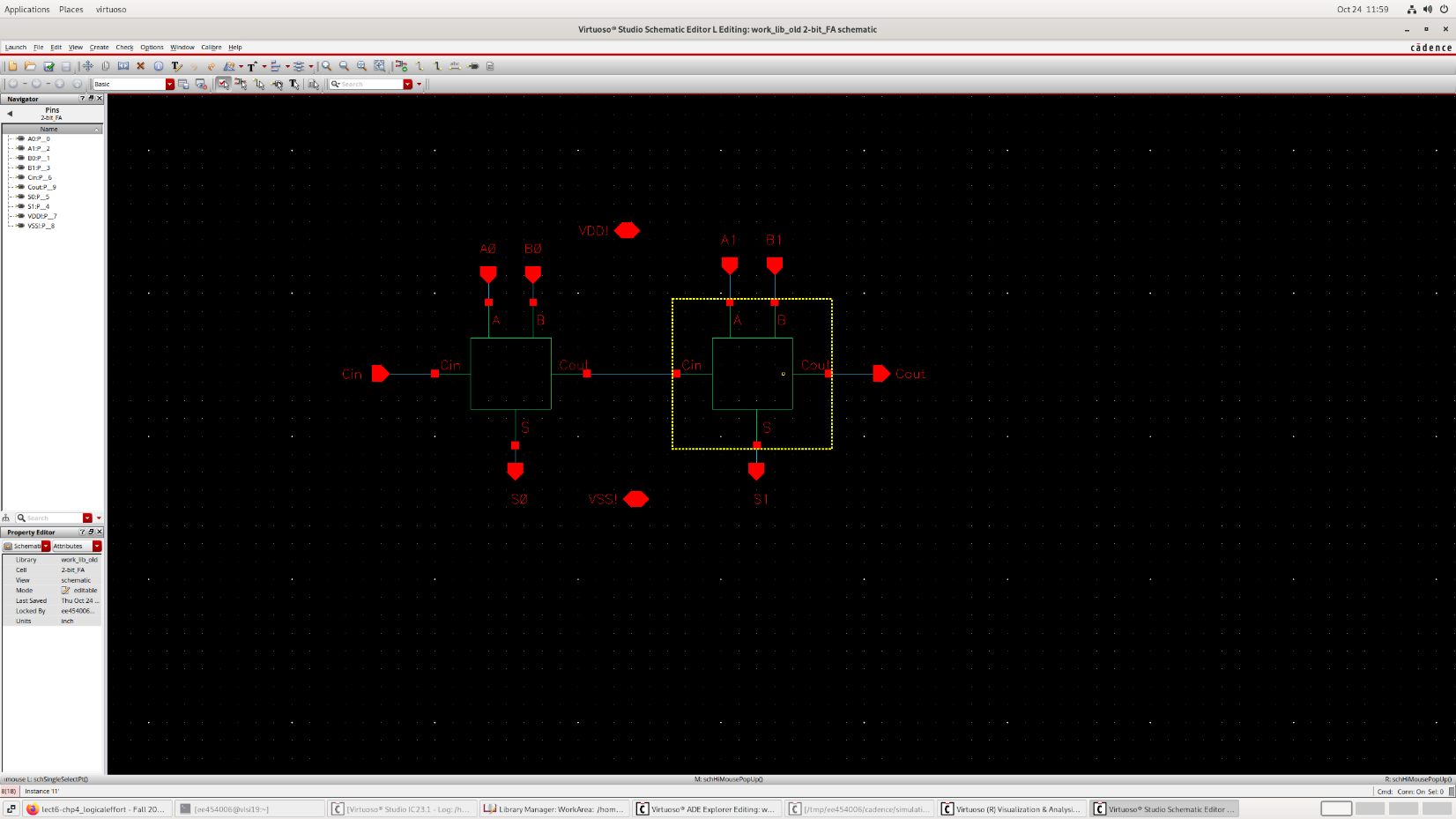
Screens screenshot of a computer

Description automatically generated

A computer screen shot of a computer program

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1. bit FA:



1. **CONCLUSION**

This lab overall wasn’t that bad to implement since I had already made the XOR2, although I did run into a few challenges. First of all, deciding how to make the 1-bit FA from the truth table simplification was difficult but with time I think I figured it out. I overcame this by doing research on how to make it and testing different designs to see which one would work best for the lab. Another challenge I faced was confirming the 2-bit FA waveform to be correct, I couldn’t decide if the output I had received was correct and after doing some math on the outputs I seemed to have a working 2-bit FA. Something I could’ve done to make the designs better was to adjust the widths of the transistors to have equal propagation delays, but I didn’t have enough time to implement this in my designs.